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For

VOLTAGE-CONTROLLED OSCILLATOR CIRCUIT FOR DIRECT MODULATION

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VOLTAGE-CONTROLLED OSCILLATOR CIRCUIT FOR DIRECT MODULATION

FIELD OF THE INVENTION

[0001] The present invention relates generally to frequency modulation and more particularly to an improved voltage-controlled oscillator circuit (VCO) to effect direct modulation.

BACKGROUND OF THE INVENTION

[0002] A phase-locked loop (PLL) circuit is a type of control loop in which both the phase and frequency of a local oscillator is maintained close ("locked") to the phase and frequency of an external reference signal. PLL circuits are implemented in a wide variety of electronic devices including frequency synthesizers for transceivers in radio communication devices. PLL circuits are attractive in modulation applications due to their combination of controllable modulation and stable and adjustable carrier frequency.

[0003] **Figure 1** shows a block diagram of a typical PLL circuit in accordance with the prior art. The PLL circuit 100, shown in **Figure 1**, includes five basic components: a phase and frequency comparator (phase and frequency detector) 105, a charge pump 106, a loop filter 110, a voltage controlled oscillator (VCO) 115, and a clock divider (frequency divider) 120. The components are connected in a feedback configuration as shown in **Figure 1**. The phase detector 105 compares the phase and frequency of the input reference clock signal 102 with the phase and frequency of the feedback VCO signal 108 through the clock divider 120. The charge pump 106 provides a DC output signal 103 proportional to the phase and frequency difference of the two signals. The VCO circuit generates a frequency proportional to its input voltage. The output voltage

of the charge pump 106 is used to adjust the VCO 115 until the difference in phase and frequency between the two signals is very small.

[0004] The VCO may be used to implement a frequency modulation scheme. For example, a VCO circuit typically used in IQ modulation includes a series of variable capacitors for coarsely tuning the center output frequency and a varactor (voltage controlled capacitor) for finely tuning the center output frequency to the desired frequency. For IQ modulation the VCO circuit is used to set the carrier frequency. Then IQ modulation circuitry is used to modulate the center frequency with a waveform that slightly changes the carrier's frequency. The in-phase (I) portion and the quadrature (Q) portion of the modulating signal contain the transmitted data. For such modulation techniques, in which the VCO only acts to set the center frequency, there is no stringent requirement of linearity for the VCO circuit gain (KVCO). Therefore, the use of a varactor, that produces a linear voltage/frequency characteristic over only a small range, does not present a problem.

[0005] In contrast, direct modulation requires a very linear KVCO for greater ranges. For direct modulation, digital data is sent to the PLL, and then based upon this data, a control voltage is generated that includes both the center frequency and the data signal. The control voltage of the VCO is being modulated so modulation depends solely on the linearity of the VCO. With direct modulation the modulating wave shifts a center output frequency between predetermined values, i.e., two different carrier frequencies are used to represent zero and one, respectively. The carrier frequencies, f_0 and f_1 (representing 0 or 1) are typically shifted in like amount from a center frequency. For example, for a wireless standard having 79 channels in a frequency range of 2402Mhz – 2480Mhz with

each channel separated by 1Mhz the center frequencies may be equal to 2402Mhz + nMhz (n= 0 to 78). For example, for center frequency f_c equal to 2402 Mhz, f_0 equals 2402 Mhz minus some value (e.g., 160Khz) and f_1 equals 2402 Mhz plus a corresponding value. Of course the carrier frequencies are not individual frequencies, but cover a range of frequencies depending on the type of modulation and the signal waveform. Therefore, f_0 may range from f_c – 140Khz to f_c – 170Khz and f_1 may be range from f_c + 140Khz to f_c + 170Khz. For such a modulation scheme a linear KVCO is required over a much larger range compared with other modulation techniques (e.g., IQ modulation).

[0006] Another drawback of the prior art VCO (in addition to the small range of KVCO linearity) in terms of implementing direct modulation is that the varactor's voltage-capacitance curve is linear in only a very small region. The bias voltage required for the varactor to operate in the linear range may be outside the voltage range of the VCO power supply.

[0007] A further consideration is external noise. Typically, for radio communication applications, the bandwidth of loop filter 110 is very small. A small loop filter bandwidth necessitates large capacitance and resistance values. These are usually too big to be implemented as integrated components and so the loop filter may be implemented externally (i.e., external to the PLL chip). The signal may pick up some noise as it passes from the PLL chip through the bonding wire and PCB and back to the PLL chip.

[0008] A VCO that addresses these issues may be significantly better for implementing a direct modulation scheme.

SUMMARY OF THE INVENTION

[0009] A voltage-controlled oscillator (VCO) circuit is described for a fractional-*n* PLL circuit (i.e., having a fractional-*n* frequency divider). The VCO circuit includes a variable capacitor for coarse tuning and a varactor for fine tuning. The variable capacitor provides a plurality of capacitance values, each capacitance value corresponds to a distinct frequency band. The capacitance values are selected so as to provide a frequency/voltage characteristic for the VCO that is sufficiently linear to implement direct modulation for the frequency band. A capacitor is placed in series with the varactor to linearize the frequency/voltage characteristic of the varactor. The series capacitor value is sufficient to implement direct modulation for a specified channel frequency within the frequency band.

[0010] Other features and advantages of the present invention will be apparent from the accompanying drawings, and from the detailed description, that follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The present invention is illustrated by way of example, and not limitation, by the figures of the accompanying drawings in which like references indicate similar elements and in which:

[0012] **Figure 1** shows a block diagram of a typical PLL circuit in accordance with the prior art;

[0013] **Figure 2** illustrates a VCO circuit in accordance with one embodiment of the present invention;

[0014] **Figure 3** is a graphical representation of exemplary KVCO values for varying capacitance values;

[0015] **Figure 4** is a graphical representation of exemplary capacitance/voltage values for a typical varactor;

[0016] **Figure 5A** is a graphical representation of exemplary voltage/capacitance values for a typical varactor in accordance with the prior art; and

[0017] **Figure 5B** is a graphical representation of exemplary voltage/capacitance values for a varactor in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0018] A VCO circuit is described for implementing a direct modulation scheme. An embodiment of the invention provides a bank of switchable capacitors used to stringently control the gain of the VCO (KVCO). The capacitors provide the stringent control necessary for direct modulation. For one embodiment a linear capacitor is used to linearize the frequency/capacitance response of a single varactor. A reference voltage is used to bias the varactor diode to ensure operation within a linear range. For one embodiment the input voltages to the VCO are across a resistance value sufficient to dampen noise picked up through an external loop filter.

[0019] It is an intended advantage of one embodiment of the present invention to provide a controlled voltage/frequency response of sufficient linearity to allow implementation of direct modulation. It is another intended advantage of one embodiment of the present invention to provide a linearized capacitance/voltage response of a varactor within a desirable voltage range. It is a further intended advantage of one embodiment of the present invention to reduce the effect of external noise on the VCO output.

[0020] In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

[0021] **Figure 2** illustrates a VCO circuit in accordance with one embodiment of the present invention. The VCO circuit 220, shown in Figure 2, includes an inductor 225, a bank of switchable capacitors 230 (e.g., bank of four capacitors C_0-C_3), a series capacitor 235, and a varactor 240. The frequency of VCO circuit 220 is determined by the inductance and capacitance of the circuit (i.e., the frequency is inversely proportional to square of the product of the inductance and effective capacitance). With the inductor 225 set to a fixed value, the frequency of the VCO circuit may be tuned by adjusting the capacitance. The bank of capacitors 230 may be used to coarsely tune the frequency. For direct modulation it is critical that the frequency voltage characteristic be linear. For one embodiment, the values of each capacitor may be binary weighted. For example $C_1 = 2C_0$, $C_2 = 4C_0$, and $C_3 = 8C_0$. Each capacitor has a binary switch D_0-D_3 that allows the capacitor to be turned on or off. The four binary switches allow for 16 values of capacitance. The 16 values of capacitance may be chosen to provide a linear response over a much broader range of frequencies than the range of interest. For example, the 16 capacitance values may cover a frequency range of 2200Mhz to 2700Mhz for a system utilizing a frequency range of 2402Mhz to 2480Mhz. This is done to account for the tolerance values of the passive components. For such a system, three of the 16 capacitance values may cover the frequency range of 2402Mhz to 2480Mhz with each covering approximately 27Mhz.

[0022] **Figure 3** is a graphical representation of exemplary KVCO values for varying capacitance values. Graph 300, shown in **Figure 3** illustrates several points about the KVCO graph of a VCO circuit: The KVCO graph is linear for some voltage range (e.g., V_1-V_2). The corresponding frequency of the linear region depends upon the capacitance

value. And capacitance values may be selected so that the linear regions overlap in frequency. For example, the linear region corresponding to a capacitance value of $8C_0$ may cover a frequency range of 2400 Mhz – 2430 Mhz while the linear region corresponding to a capacitance value of $7C_0$ may cover a frequency range of 2425 Mhz – 2455 Mhz and the linear region corresponding to a capacitance value of $6C_0$ may cover a frequency range of 2450 Mhz – 2485 Mhz. Thus, the selected capacitance value determines the frequency band and the bank of capacitors 230 may be used for coarse tuning.

[0023] The varactor 240 may be used for fine tuning and also direct modulation. The capacitance of the varactor is determined by the control voltage, V_{con}. A change in the control voltage causes a change in the capacitance value of the varactor, which in turn changes the circuit frequency. In typical prior art VCO circuits the small linear range of the varactor is not a problem because the circuit is being tuned to a single desired center frequency. In contrast, for direct modulation a larger linear range is necessary because modulation is done for multiple channels that are near each other (e.g., 1Mhz spacing between channels).

[0024] **Figure 4** is a graphical representation of exemplary frequency/voltage values for a typical varactor. Graph 400, shown in **Figure 4**, shows that the frequency/voltage graph of the varactor is linear for only a small region. Also the slope of the linear region is quite high. Series capacitor 235, added to VCO circuit 220 in series with varactor 240, serves to linearize the frequency/voltage graph of the varactor and reduce the slope. The varactor frequency/voltage response is linearized to the extent necessary to implement

direct modulation. For one embodiment, series capacitor 235 is a metal-insulator-metal (MIM) type capacitor having a very linear capacitance/frequency characteristic.

[0025] Of course the linearization of the varactor frequency/voltage response reduces the frequency ranged covered by the varactor, but the covered frequency range is increased through use of the variable capacitance of the bank of capacitors 230 as described above. The voltage across the varactor diode must be biased with a certain voltage to obtain a linear response. However the required voltage may be outside the range of the control voltage. **Figure 5A** is a graphical representation of exemplary voltage/capacitance values for a typical varactor in accordance with the prior art. Graph 500A, shown in **Figure 5A**, shows that the variable capacitance value of the varactor corresponds to an applied voltage between V_1-V_4. The linear range (i.e., V_{app} between V_2-V_3) may be a negative voltage that may not be available. The reference voltage, V_{Ref}, is a constant value that can be used to set the desired DC bias for the varactor diode to operate in a specified region. **Figure 5B** is a graphical representation of exemplary voltage/capacitance values for a varactor in accordance with one embodiment of the present invention. Graph 500B, shown in **Figure 5**, shows the linear range (V_2-V_3) shifted so that the required V_{app} is a more convenient value. Capacitor 235 may be used to isolate the DC voltage of reference voltage, V_{Ref}, to node 236. Thus series capacitor 235 serves to linearize the varactor frequency/voltage response and also to allow the varactor diode to be biased at a desired bias point.

[0026] As described above the loop filter may be implemented externally necessitating the signal to leave the PLL chip and traverse portions of the PCB. For one embodiment the VCO circuit 220 also contains resistors 246a, 246b, and 246c. These

resistors help to dampen any noise that may be picked up as the signal leaves the PLL chip and returns.

[0027] In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense.